WHAT IS CLAIMED IS:

1. A signal processing device utilizing partial response maximum likelihood detection, comprising:

an iterative decoder which detects a signal from a partial response equalized sample value sequence, utilizing iterative decoding, the iterative decoder having a plurality of cascade-connected decoder units, each of the decoder units including a soft-decision Viterbi detector which outputs soft-decision values from a sample value sequence input to each of the decoder units;

a partial response waveform generator which generates a digital value sequence of an expected partial response waveform based on an output of the soft-decision Viterbi detector included in a predetermined one of the decoder units, the predetermined decoder unit being other than a final-stage decoder unit;

a flag generator which generates flag information indicative of whether reliability of the digital value sequence generated by the partial response waveform generator is low or high, based on the output of the soft-decision Viterbi detector included in the predetermined decoder unit;

an error detector which detects error values in the partial response equalized sample value sequence, the error detector utilizing the digital value sequence

generated by the partial response waveform generator, as a digital value sequence of a reference waveform for feedback control of a predetermined control target, the reference waveform being referred to for error value detection; and

an error output controller which controls output of the error values detected by the error detector in accordance with a state of the flag information generated by the flag generator.

2. The signal processing device according to claim 1, wherein the predetermined decoder unit is a first-stage decoder unit included in the plurality of decoder units.

3. The signal processing device according to claim 1, wherein the flag generator includes:

an absolute value converter which converts, into an absolute value, a soft-decision value output from the soft-decision Viterbi detector included in the predetermined decoder unit;

a comparator which compares an output of the absolute value converter with a predetermined threshold value; and

a flag setting unit which sets a state of the flag information in accordance with a comparison result of the comparator.

4. The signal processing device according to claim 3, wherein:

the flag generator further includes a delay circuit which delays the comparison result of the comparator by one of one sampling period to a number (n-1) of sampling periods, n indicating a sampling period in which influence of the partial response equalized sample value sequence exerts; and

the flag setting unit sets the flag information in a particular state indicating that the reliability of the digital value sequence generated by the partial response waveform generator is low, during a period in which at least one of the comparison result of the comparator and an output of the delay circuit indicates that the output of the absolute value converter is lower than the threshold value, the output of the delay circuit being generated during the one of the one sampling period to the number (n-1) of sampling periods.

5. The signal processing device according to claim 4, wherein the delay circuit includes a number (n-1) of delay elements connected by cascade connection, a first-stage one of the number (n-1) of delay elements having an input terminal connected to an output terminal of the comparator, the number (n-1) of delay elements delaying respective inputs by one sampling period.

6. The signal processing device according to claim 5, wherein the number (n-1) of delay elements are

flip-flops which hold their respective inputs for one sampling period in synchrony with a sampling clock.

7. The signal processing device according to claim 1, wherein the partial response waveform generator includes:

a hard-decision unit which binarizes a soft-decision value output from the soft-decision Viterbi detector included in the predetermined decoder unit, in accordance with polarity of the soft-decision value, thereby outputting a binary sequence; and

a convolution integrator which executes convolution integration of the binary sequence output from the hard-decision unit and predetermined partial response values, the convolution integrator outputs a result of the convolution integration as a digital value sequence of an expected partial response waveform.

8. The signal processing device according to claim 7, wherein the convolution integrator includes:

a number (n-1) of delay elements connected by cascade connection, a first-stage one of the number (n-1) of delay elements having an input terminal connected to an output terminal of the hard-decision unit, the number (n-1) of delay elements delaying respective inputs by one sampling period;

a first multiplier which multiplies an output of the hard-decision unit by a predetermined parameter

value;

a number (n-1) of second multipliers which multiply outputs of the number (n-1) of delay elements by respective parameter values uniquely assigned to the number (n-1) of delay elements; and

an adder which adds an output of the first multiplier and outputs of the number (n-1) of second multipliers.

9. The signal processing device according to claim 1, wherein the error output controller sets a to-be-output error value to a value lower than a detection result of the error detector, during a period in which the flag information generated by the flag generator indicates that the reliability of the digital value sequence generated by the partial response waveform generator is low.

10. The signal processing device according to claim 1, wherein the error output controller sets a to-be-output error value to 0, regardless of a detection result of the error detector, during a period in which the flag information generated by the flag generator indicates that the reliability of the digital value sequence generated by the partial response waveform generator is low.

11. The signal processing device according to claim 1, wherein one of a signal gain, a signal offset, asymmetry of a signal waveform, timing recovery is

the control target subjected to feedback control based on the error values whose output is controlled by the error output controller.

12. The signal processing device according to claim 1, further comprising:

a variable gain amplifier which adjusts an amplitude of a read analog signal;

an analog filter which filters an analog signal output from the variable gain amplifier;

an offset compensator which receives the analog signal filtered by the analog filter and compensates an offset of the analog signal;

an A/D converter which converts an analog signal, output from the offset compensator, into a quantized discrete-time sample value sequence in synchrony with a sampling clock;

a digital filter which equalizes the quantized discrete-time sample value sequence output from the A/D converter in a desired response direction, and outputs a partial response equalized sample value sequence;

an automatic gain controller which feedback-controls a gain of the variable gain amplifier such that the variable gain amplifier maintains the amplitude of the read analog signal constant;

an offset controller which feedback-controls offset compensation by the offset compensator;

a timing recovery controller which

feedback-controls timing of the sampling clock used for sampling by the A/D converter; and

an equalized characteristic controller which feedback-controls an equalized characteristic of the digital filter,

wherein at least one of the automatic gain controller, the offset controller, the timing recovery controller and the equalized characteristic controller includes a combination of the partial response waveform generator, the flag generator, the error detector and the error output controller.

13. The signal processing device according to claim 1, wherein the soft-decision Viterbi detector utilizes a soft-output Viterbi algorithm which computes, as soft-decision values, a logarithmic ratio of a posterior probability of an input sample value sequence.

14. A disk drive for writing and reading data to and from a disk, using a head, comprising:

a head amplifier which amplifies an analog signal read by the head; and

a signal processing device which converts the analog signal, amplified by the head amplifier, into a partial response equalized sample value sequence, and decodes original data from the partial response equalized sample value sequence, the signal processing device including:

an iterative decoder which detects a signal from a partial response equalized sample value sequence, utilizing iterative decoding, the iterative decoder having a plurality of cascade-connected decoder units, each of the decoder units including a soft-decision Viterbi detector which outputs soft-decision values from a sample value sequence input to each of the decoder units;

a partial response waveform generator which generates a digital value sequence of an expected partial response waveform based on an output of the soft-decision Viterbi detector included in a predetermined one of the decoder units, the predetermined decoder unit being other than a final-stage decoder unit;

a flag generator which generates flag information indicative of whether reliability of the digital value sequence generated by the partial response waveform generator is low or high, based on the output of the soft-decision Viterbi detector included in the predetermined decoder unit;

an error detector which detects error values in the partial response equalized sample value sequence, the error detector utilizing the digital value sequence generated by the partial response waveform generator, as a digital value sequence of a reference waveform for feedback control of

a predetermined control target, the reference waveform being referred to for error value detection; and

an error output controller which controls output of the error values detected by the error detector in accordance with a state of the flag information generated by the flag generator.

15. A signal processing method for feedback control of a predetermined control target, for use in a disk drive which decodes data from a sample value sequence obtained by sampling an analog signal read from a disk, utilizing partial response maximum likelihood detection, the disk drive including an iterative decoder which detects a signal from a partial response equalized sample value sequence, utilizing iterative decoding, the iterative decoder having a plurality of cascade-connected decoder units, each of the decoder units including a soft-decision Viterbi detector which outputs soft-decision values from a sample value sequence input to each of the decoder units, the signal processing method comprising:

generating a digital value sequence of an expected partial response waveform based on an output of the soft-decision Viterbi detector included in a predetermined one of the decoder units, the predetermined decoder unit being other than a final-stage decoder unit;

generating flag information indicative of

whether reliability of the digital value sequence of the expected partial response waveform is low or high, based on the output of the soft-decision Viterbi detector included in the predetermined decoder unit, generation of the flag information being parallel to generation of the digital value sequence;

detecting error values in the partial response equalized sample value sequence by utilizing the generated digital value sequence as a digital value sequence of a reference waveform used for feedback control of a predetermined control target; and

controlling output of the detected error values in accordance with a state of the generated flag information.